



Docket No.: R2180.0188/P188  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re Patent Application of:  
Takamitsu Yamada et al.

Application No.: 10/763,255

Confirmation No.: 7512

Filed: January 26, 2004

Art Unit: 2138

For: SEMICONDUCTOR INTEGRATED  
CIRCUIT AND SCAN TEST METHOD  
THEREFOR

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Examiner: Phung M. Chung

**AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION**

MS Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

**INTRODUCTORY COMMENTS**

In response to the Office Action dated March 14, 2006, please amend the above-identified U.S. patent application as follows:

**Amendments to the Abstract** begin on page 2 of this paper.

**Amendments to the Claims** are reflected in the listing of claims which begins on page 3 of this paper.

**Remarks/Arguments** begin on page 9 of this paper.